Design of a High Performance Three-Phase Induction Motor Drive System with Current Limit Strategy

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***Abstract*— In this paper to compensate for the current stress for Induction Motor Drive , a novel current limit strategy with minimized DC-Link capacitor is proposed. In order to avoid excessive pumping up in dc-link voltage during the occurrence of a fault, the conventional all-turn-off current limit logic is replaced and there by eliminating the reversal dc-link current. For this a low cost fault tolerant control strategy, based on a quasi-cycloconverter method is proposed as a potential solution for overcoming the reversal dc-link current. In this configuration, along the PWM drive, the three-phase Induction motor terminals are connected to the ac supply mains through a group of back-to-back connected SCRs which can even provide a speed control at selectable frequencies by controlling the switching patterns of a SCR switches by adjusting the frequency and the firing angles of the SCRs . The proposed design stands out as it is used for mitigating all driver faults along with elimination of reversal dc-link current with very minimal hardware modifications and there by providing system compactness, reliability as well as cost effectiveness. This proposed control strategy is verified by simulating using the software Matlab-Simulink and desirous waveforms for DC link current and voltage along with speed torque waveforms are obtained.**

***Index Terms*— Induction motor, Inverter switch-faults, current limit strategy, fault mitigation technique, dc-link capacitor, pumping-up voltage, reversal dc-link current.**

I. INTRODUCTION

Polyphase induction motors due to it's simple construction, ruggedness and low cost have been the main prime movers for industrial and manufacturing processes as well as numerous propulsion applications. This has escalated the importance and the significance of developing rigorous fault mitigation techniques or fault tolerant for such types of systems. Inorder to maintain the smooth operation of Induction Motor drives the stability of DC Link capacitor is of great importance. In the event of a faulty condition in the inverter switches under conventional current limit strategy bumping up of DC Link voltage occurs which is usually compensated by using dc link with sufficient capacitance which not only adds to the increase in the system volume and cost but also causes degradation of system reliability.

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The widespread use of ac motor systems in numerous critical industrial, manufacturing, and transportation applications that involve systems such as fans, blowers, compressors, pumps, elevators and escalators, assembly lines, transport and conveyor belt systems showcases the importance of ensuring a continuous, almost disturbance-free operation and a gentle, judder-free operation and thereby raising need for the reliability of a motor drive system . In order to minimize the cost as a consequence of system redundancy which was conventional adopted as a means of fault mitigation, a lot of attention has been focused on developing intelligent fault mitigation control methods, along with the appropriate modifications to the three-phase Induction motor drives. Accordingly, such fault tolerant capabilities will entail the reduction in maintenance costs as well as prevention of reversal of DC link current which will thereby makes the system compact along with providing higher reliability.

The main thrust of this work is divided into six parts. Session II first focuses on analysis different types of Inverter switch faults and its effects on motor performance. The conventional fault mitigation techniques is presented in section III. Section IV focus on the proposed fault mitigation technique along with it's control strategy and simulation results to validate the performance under any possible faulty conditions using the software Matlab-Simulink is presented in section V followed by conclusions in section VI is presented in this paper

II. TYPES OF .INVERTER SWICH FAULTS

The most common types of drive system faults is the loss of a power transistor switch in one of the legs of the inverter which can be caused by either an open-circuit or short-circuit.. Based on the studies and literature surveys conducted the major causes for fault occurrences and its percentage of failure rates,on drives are given in Table I. As one can observe therein, the power semiconductor faults account for around 35% of all faults. In fact, this percentage can be higher if one were to take into account the control circuit faults given in Table I. Such faults may be caused by inverter switches misfiring due to defects in control circuit elements accordingly, this results in gate-drive open faults, and consequently leads to transistor open-circuit switch faults.

TABLE I :
Percentage of component failures in AC Drives

Major Components	% Of Failures
Power Converter Circuits	53
Control Circuits	38
DC Link Capacitor	60
Power Transistor	31
Diodes	3

External Auxiliaries	9
Others	6

The open-circuit transistor switch fault is commonly due to either a malfunction in one of the PWM output ports of the controller or a malfunction in the gate drive. On the other hand, the short circuit transistor switch fault can be caused by a breakdown of the snubber circuit or a loose wire, resulting in a short-circuit fault. The studies demonstrate that the short-circuit SCR fault produces undesired fault response on motor performance with unbalanced, high starting currents which accordingly result in high starting torque pulsations, whereas the open-circuit SCR switch fault results in no starting torque from the motor, hence it constitutes a total failure of motor starting which leads to reversal of DC link current as thereby inducing fluctuations in DC link Current and voltages and thereby effecting the system performance. Therefore, the need to develop fault-tolerant systems is highly desirable

III. .CONVENTIONAL FAULT MITIGATION TECHNIQUES

There are various limp-home strategies for three-phase ac motor-drive systems under inverter switch faults. However the most commonly adopted methodology is by using the concepts of parallel redundancy. This topology is capable of providing fault tolerance to a transistor open-circuit or short circuit switch fault. The operating principal behind this conventional topology is that , when either a transistor open-circuit or short-circuit switch fault has been detected and diagnosed, the faulty transistor switch will be first isolated, and the fourth inverter leg will be activated for usage by turning-on the associated triac as given in Fig 1. and Fig2.

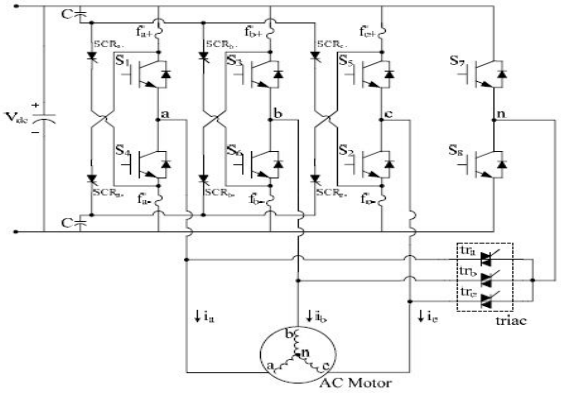

Fig 1: Pre-fault configuration.

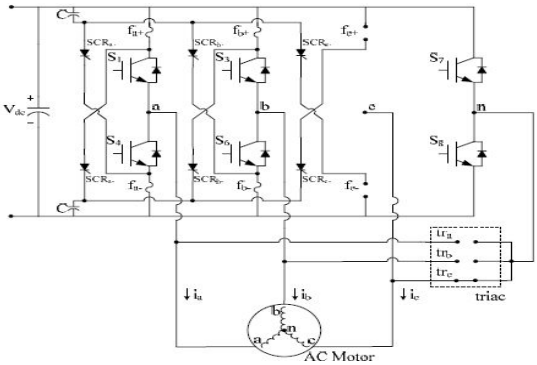

Fig 2: Post-fault configuration.

In this topology as all three phases of the motor are connected to the inverter during the pre- and post-fault operations, the current amplitude in each of the phases remains the same in order to ensure a smooth torque production driver circuits, To further explore the possibility of cost reduction as a consequence of system redundancy, various reduced switch-count converter topologies for three-phase ac motor-drive systems have been developed with high reliability due to the reduced number of power switching components. However in these fault mitigation topologies still exists certain demerits like accessibility to the motor neutral is the required, which is normally not provided by motor manufacturers and oversizing the dc capacitors and doubling the dc link voltage due to reverse flow of DC link current. So this ensures the need for intelligent fault mitigation control techniques which prevents reversal of DC link current and there by ensures stability of DC link voltage and there by ensures continuous and disturbance free operations during critical applications

IV. PROPOSED FAULT MITIGATION TECHNIQUE

A. Pwm Inverter Switching

A schematic of the drive inverter circuit is shown here in Fig 3 . It consists of six power transistors connected with six anti-parallel diodes (S1 ~ S6). The development of the PWM inverter can be greatly simplified by using the averaged switching function model. This is due to the fact that the PWM switching frequency is much larger than the power frequency of the desired inverter ac output voltages. Accordingly, one can assume almost sinusoidal (rippleless) output waveforms since the higher-order frequency time harmonics can be easily filtered out by the inherent low-pass filtering capability of the motor windings, and the lower-order harmonic effects due to winding layouts and core saturations are neglected during the analysis process

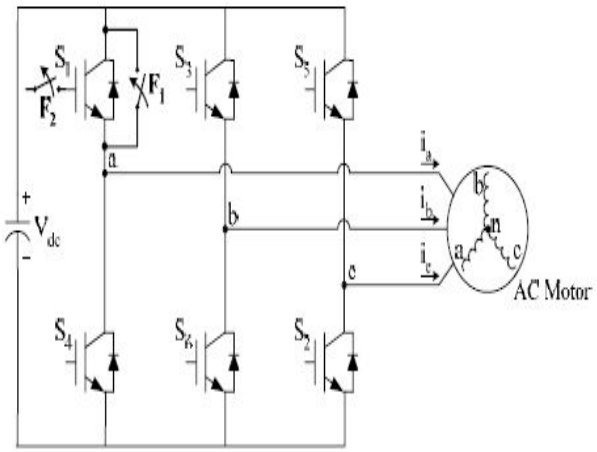

Fig 3 : Inverter drive Circuit

Mathematical the switching function of each of the corresponding switches, S_1 to S_6 are represented as $H_j(t)$ = 1,2,3,4,5,6 respectively. Furthermore, $H_j(t) = 1$ when a switch is turned-on, and $H_j(t) = 0$ when a switch is turned-off.

The switching states of H_1, at any given time instant, depend on the comparison outcome between the reference signal, V_{ref} and the carrier (or triangle) signal, $V_{carrier}$

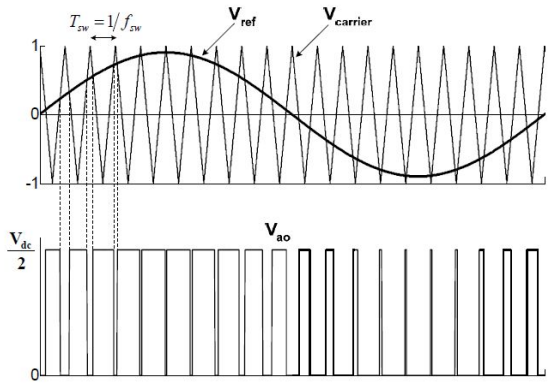

Fig 3 : PWM switching function, H_1, of switch, S_1

Here, the reference signal, V_{ref} ,represents the duty ratio, da, that varies in a sinusoidal fashion which also represents the desired fundamental inverter output ac voltage waveform. On the other hand, the carrier signal, V_{tri} is a triangle wave that varies between -1 and 1 with a switching frequency, f_{sw}

Proposed Fault Mitigation Technique And Control Strategy

The main idea leading to the development of the present approach as a potential solution for motor-drive inverter switch fault mitigation was attributed to the discovery that by proper control of the SCRs, in a specific switching pattern can produce a set of three-phase positive-sequence voltages with a fundamental frequency other than the input supply frequency. It was this specific discovery that led to a finding a potential remedial solution for inverter faults, by connecting the three phase SCR bridge whose configuration is shown in Fig 5 in parallel with the drive. In the event of a fault, the drive will shut down by its own fault protection system, and the SCR bridge will bypass the faulty drive to continue operation of the motor using the present control method

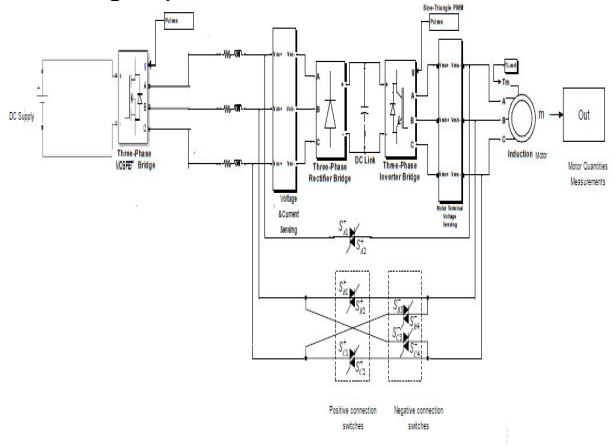

Fig 5 : Block Diagram Of The Proposed Fault Mitigation Scheme.

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The present topology structure and its operating principles can be considered as similar to an ac-to-ac frequency changer . The basic function of a cycloconverter is to convert directly the incoming frequency to some different output frequency. For most practical purposes, the maximum attainable useful output frequency is less than the input frequency which is the only limitation. The operation of a cycloconverter is carried out by controlling the switching patterns of SCR switches connected directly between the input ac system and the motor. A typical three-phase cycloconverter consists of 6 SCR switches for each phase, resulting in a total of 18 SCR switches, whereas in the proposed control strategy uses only 10 SCR switches and hence considered as a quasi-cycloconverter ,or a reduced-switch-count cycloconverter, for three-phase modes of operation.

Furthermore, by controlling the frequency and depth of phase modulation of the firing angles of the SCRs, it is possible to control the frequency and amplitude of the fundamental component of the output voltages. Hence, the operation of the present topology resembles, to a certain extent, the operation of a typical volts per- hertz PWM drive and thereby provides speed control at selectable frequencies.

The control logic (flowchart) of the present topology is illustrated in Fig 6. The same control logic is also applied to all three phases. It first begins by sensing the phase-*a* supply mains, V_{ref} , and applying the zero-crossing detection scheme to the measured signal. When a zero crossing of the voltage, V_{SA} , is detected, a phase-delayed angle counter will be initiated to begin counting. Once the phase-delayed angle counter has reached the value of the angle, α , a single firing pulse is generated by either the positive pulse generator or the negative pulse generator depending upon the nature of the zero crossing.

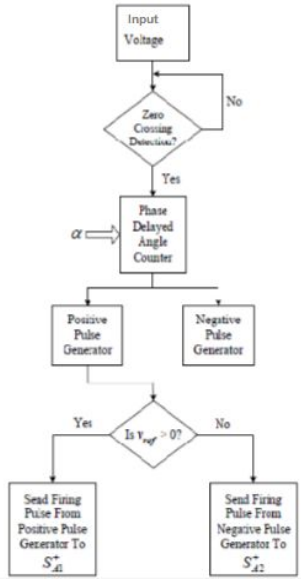


Fig 6 :Flow Chart of the Proposed Control Scheme

If the zerocrossing occurs during the instant when the polarity of the voltage changes from negative to positive, the positive pulse generator will be selected, and vice versa. Once a train of pulses has been generated, the last and crucial step is to decide the proper instant of triggering the SCRs, S_{A1}^+ and S_{A2}^+. This is carried out by monitoring the polarity of the reference waveform, V_{ref} , for phase-*a*. If $V_{ref} > 0$ the firing pulse generated by the positive pulse generator is sent to the gate of S_{A1}^+ for the turn-on, while S_{A2}^+ remains off. On the contrary, if $V_{ref} < 0$, S_{A2}^+ will be turned-on by the firing pulse generated by the negative pulse generator, and S_{A1}^+ will be in its turn-off state

V. SIMULATION RESULTS

The The circuit simulation results of the inverter-motor system using the proposed fault tolerant topology based configuration is presented. The simulation work was carried out using a commercially available circuit simulation software package, namely Matlab-Simulink.

Practical application considerations and opportunities for practical use of the present conceived design are also considered while simulating. This is in order to highlight the potentials of the present design as a possible fault-tolerant solution for drive-related faults, as well as the potential utilization of this type of design as a low-cost, moderate-performance drive with high reliability and thereby preventing reversal of DC Link current and hence obtaining a compact system.

The Matlab-Simulink simulation model of the power circuit structure of the induction motor drive system and its control logic is depicted in Fig 7 and Fig 8. The motor under investigation is a 2-hp, 460-volt, 50-Hz, 4-pole, three-phase squirrel-cage induction motor with the following machine parameters Stator resistance and inductance as R_S = 3.850Ω and L_s =17.5594mh , Rotor resistance and inductance as R_r = 2.574 Ω and L_r =17.5594mh, Mutual Inductance L_m = 0.372674 H. Also we have used a carrier based sine-triangle PWM controller with modulation index m_a = 0.4 and switching frequency = 500Hz.

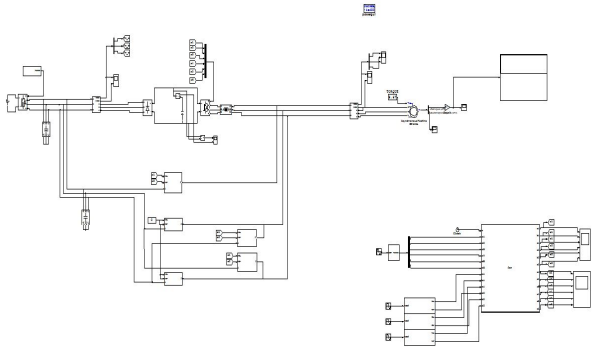


Fig 7 : Simulation Diagram Of Proposed Topology

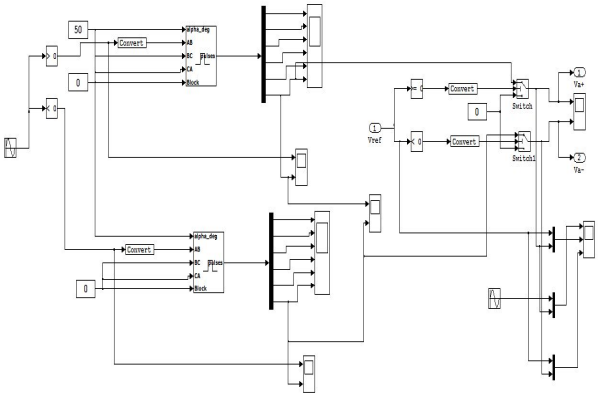


Fig 8 : Simulation Diagram For Control Logic

The waveforms obtained for Phase Voltages , DC Link current DC link voltage speed as well as torque without implementation of fault mitigation technique as well as with implementation of fault mitigation technique is given below.

As given in Fig. 9,upon the occurrence of fault at t =0.8 sec , the motor phase voltage reduces to zero subsequently, with a reversal of current in the DC Link capacitor which causes bumping up of DC Bus voltage as shown in fig 12a.and fig 13 a. Also the braking torque introduced by the dc magnetic field causes the speed to drop and the electromagnetic interactions between the resultant stator dc field and the resultant rotor fundamental rotating field introduce a pulsating torque, and subsequent speed ripples, at the fundamental power as depicted in figures 14a and 15a.

With the implementation of the proposed fault mitigation scheme, continuity in the motor operation is ensured there by preventing the reversal of DC link current in the DC link capacitor and there by providing stability to the DC Bus voltage as shown in fig 12b and fig13b. The speed and the torque waveforms obtained is also given below in fig14b and fig 15b.

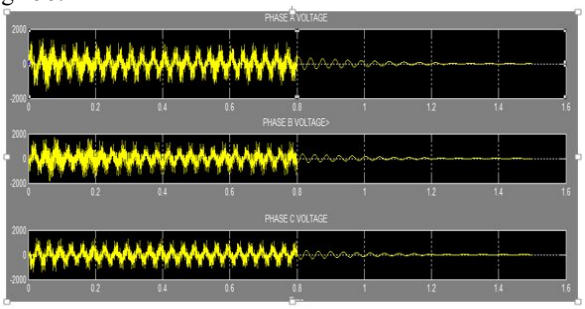


Fig 9: Phase Voltages Without Fault Mitigation Implementation

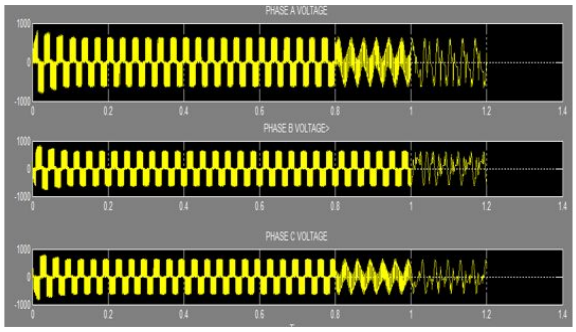
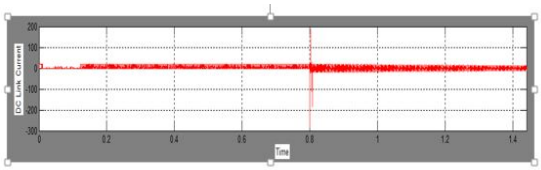
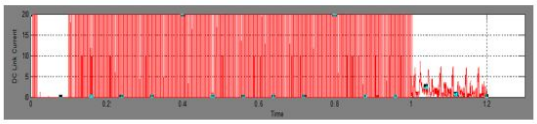


Fig 10: Phase Voltages WithFault Mitigation Implementation

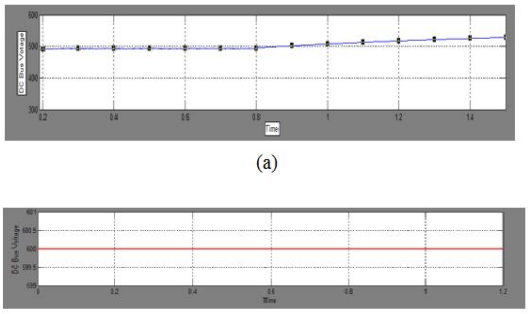


(a)



(b)

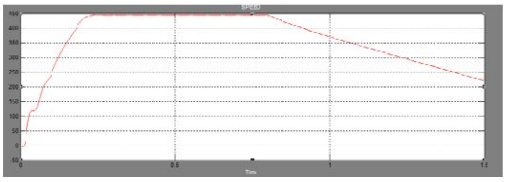
Fig 11: DC Link Current Waveforms : (a)Without fault mitigation technique (b) With fault mitigation technique



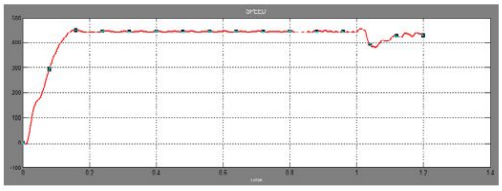
(a)

(b)

Fig 12: DC BusVoltage Waveforms : (a)Without fault mitigation technique (b) With fault mitigation technique

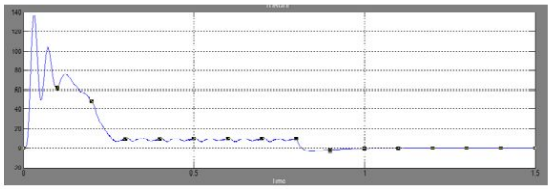


(a)

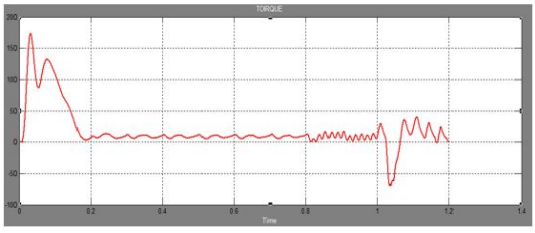


(b)

Fig 13: Motor Speed Waveforms : (a)Without fault mitigation technique (b) With fault mitigation technique



(a)



(b)

Fig 14: Motor Torque Waveforms : (a)Without fault mitigation technique (b) With fault mitigation technique

CONCLUSION

.In this paper the proposed design stands out as the proposed current limit strategy, prevents the reversal of dc-link current and thereby prevents pumping up of dc-link voltage and hence makes the system compact along with providing reliability and ensuring continuous and disturbance free motor operation by mitigating other drive –related faults that occurs in the diode –rectifier bridge or dc-link of the drive along with inverter faults with minimum hardware modifications

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